

CLAIMS

- 1 1. A semiconductor device comprising:
 - 2 a) a source, a drain and a body between the source and the drain, the body
 - 3 having a first side and a second side;
 - 4 b) a first double gate, the first double gate having a first portion adjacent to the
 - 5 body first side and a second portion adjacent to said body second side;
 - 6 c) a second double gate, the second double gate having a first portion adjacent
 - 7 to the body first side and a second portion adjacent to said body second side.
- 1 2. The semiconductor device of claim 1 wherein the body comprises a fin body
- 2 that has a width narrow enough to insure a fully depleted channel during
- 3 operation of the transistor.
- 1 3. The semiconductor device of claim 1 wherein the first double gate receives a
- 2 first control signal and said second double gate receives a second control
- 3 signal.
- 1 4. The semiconductor device of claim 1 wherein the body comprises a portion of
- 2 a silicon-on-insulator layer.

1 5. The semiconductor device of claim 1 further comprising an insulating spacer
2 between the first double gate and the second double gate.

1 6. The semiconductor device of claim 1 wherein the first body side and the
2 second body side are on opposite sides of the body.

1 7. The semiconductor device of claim 1 comprising a first insulating spacer
2 between the first portion of the first double gate and the first portion of the
3 second double gate, and a second insulating spacer between the second portion
4 of the first double gate and the second portion of the second double gate.

1 8. The semiconductor device of claim 7 wherein the first insulating spacer and
2 second insulating spacer are formed offset such that the first insulating spacer
3 and second insulating spacer are not inline across the body.

1 9. A method for forming a field effect transistor, the method comprising the
2 steps of:
3 a) providing a semiconductor substrate;
4 b) patterning the semiconductor substrate to provide a body, the body having a
5 first side and a second side;
6 c) forming a first double gate, the first double gate having a first portion
7 adjacent to the body first side and a second portion adjacent to said body
8 second side;
9 d) forming a second double gate, the second double gate having a first portion
10 adjacent to the body first side and a second portion adjacent to the said body
11 second side.

1 10. The method of claim 9 wherein the step of patterning the semiconductor
2 substrate to provide a body comprises patterning the semiconductor substrate
3 to form a fin type body.

1 11. The method of claim 9 wherein the semiconductor substrate comprise a
2 silicon-on-insulator layer and wherein the step of patterning the
3 semiconductor substrate to provide a body comprises patterning the silicon-
4 on-insulator layer.

1 12. The method of claim 9 further comprising the step of forming an insulating
2 spacer between the first double gate and the second double gate.

1 13. The method of claim 12 wherein the step of forming an insulating spacer
2 between the first double gate and the second double gate comprises forming a
3 first insulating spacer between the first portion of the first double gate and the
4 first portion of the second double gate, and forming a second insulating spacer
5 between the second portion of the first double gate and the second portion of
6 the second double gate, wherein the first insulating spacer and second
7 insulating spacer are formed offset such that the first insulating spacer and
8 second insulating spacer are not inline across the body.

1 14. The method of claim 9 further comprising the steps of forming a contact on
2 the first double gate to provide a first control signal and a contact on the
3 second double gate to provide a second control signal.

))

1 15. A transistor comprising:

2 a) a fin body formed on a substrate, the fin body having a first vertical edge

3 and a second vertical edge, and a first end and a second end;

4 b) a source formed at the first end of the fin body, and a drain formed at the

5 second end of the fin body;

6 c) a first gate structure adjacent the transistor body first vertical edge and

7 second vertical edge, the first gate structure approximate to the source; and

8 d) a second gate structure adjacent the transistor body first vertical edge and

9 second vertical edge, the second gate structure approximate to the drain.

1 16. The transistor of claim 15 further comprising a spacer between the first gate

2 structure and the second gate structure.

1 17. The transistor of claim 16 wherein the portion of the spacer adjacent to the

2 first vertical edge is offset from the portion of the spacer adjacent to the

3 second vertical edge.

1 18. The transistor of claim 15 wherein the fin body has a width narrow enough to

2 insure a fully depleted channel during operation of the transistor.

1 19. The transistor of claim 15 wherein a portion of the first gate structure adjacent
2 to the first vertical edge of the transistor body is directly opposite a portion of
3 the second gate structure adjacent to the second vertical edge of the transistor
4 body.

1 20. The transistor of claim 19 wherein the first gate structure adjacent to the first
2 vertical edge of the transistor body has a work function which is more
3 attractive to dominant charge carriers of the transistor compared to that of the
4 first gate structure adjacent to the second vertical edge of the transistor body.

1 21. The transistor of claim 20 wherein the second gate structure adjacent to the
2 second vertical edge of the transistor body has a work function which is more
3 attractive to the dominant charge carriers of the transistor compared to that of
4 the second gate structure adjacent to the first vertical edge of the transistor
5 body.

1 22. The transistor of claim 15 wherein an edge of the first gate structure adjacent
2 to the first vertical edge of the transistor body is opposite, and displaced less
3 than the body thickness from an edge of the second gate structure adjacent to
4 the second vertical edge of the transistor body
